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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,826	10/19/2001	David Patrick Magee	TI-32984	1043

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EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/082,826	MAGEE, DAVID PATRICK	
	Examiner	Art Unit	
	Khanh Tran	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-10,14-24 and 26-29* is/are rejected.

7)☒ Claim(s) *7,11-13,25,30 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/19/01 &04/14/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-4, 20, 23-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Williams U.S. Patent 5,717,620.

Regarding claim 1, Williams invention is directed to a butterfly circuits for implementing the fast Fourier transform algorithm. The fast Fourier transform transforms an input signal from time domain to frequency domain. Figure 4 illustrates a butterfly circuit, which is a modification of figure 2 prior art to compensate for bit growth. As discussed in column 2 line 65 via column 3 line 15, a bit-growth detector 39 (shown in both figures 2 and 4) monitors the inputs to the inter-pass memory 32 as to keep track of the largest value applied during any given pass. In column 3, lines 20-36, bit-growth detector 39 controls the shifter 38 to shift all multiplicands by one less than the lowest number of bits observed in any stage. In effect, the shifter 38 multiplies all values in a given pass by a power of 2 large enough to cause the pass's largest value to have only one sign bit and thereby "fill" the input port of multiplier 34, to which it is applied. In column 5 lines 50-65, Williams approach in figure 4 is rounding the results, which introduce less error than truncation. Williams teachings employ blocks 56 and 58 after multiplier 34 and shifter 38. In view of the foregoing discussion, shifter 38 performs

equivalent scaling and scaling at other stages is omitted where bit growth is absent due to characteristics of the input signal. Rounding results as taught in Williams invention corresponds to the claimed scaling step.

Regarding claim 2, in column 6, lines 1-30, Williams teaches the fast Fourier Transform butterfly circuit includes at least one digital multiplier and a plurality of digital adders. In view of the foregoing teachings, the fast Fourier Transform butterfly circuit can include more than one digital multiplier. The adders and multipliers are inherently complex adders and multipliers.

Regarding claims 3-4, in column 2, lines 25-40, the butterfly circuit of figure 2 is "radix 4" butterfly circuit.

Regarding claim 20, claim 20 is rejected on the same ground as for claim 1 because of similar scope. Furthermore, as shown in figure 1, a receiver includes a wideband digital tuner 12 for receiving digitized signals in time domain, a digital channelizer for digital signal processing for channelizing a wideband digital signal for demultiplexing multiple frequency-division multiplexed channels by fast Fourier transformation implemented as a butterfly circuit of figure 4.

Regarding claim 23, referring to figure 4, Williams discloses the fast Fourier Transform butterfly circuit including:

a bit-growth detector 39 for monitoring the inputs to the inter-pass memory 32 so as to keep track of the largest value applied during any given pass; see column 2, lines 64-67;

referring to figure 4, a third adder for summing the digitized signal input magnitudes for N points to provide a total magnitude summation;

first adder 40 and second adder 46 for performing an input magnitude summation on processing stages;

the bit-growth detector 39 for controlling the shifter 38 to shift all multiplicands by one less than the lowest number of bits observed in any single stage. In view of that, the shifter 38 performs scaling at stages where bit growth is present.

Regarding claim 24, the bit growth detector 39 monitors the number of sign bits, and keeps tracks of the lowest number of sign bits for any input. Hence, keeping track of lowest number of sign bits corresponding to the claimed scaling values stored.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 5-6, 16-19, 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams U.S. Patent 5,717,620.

Regarding claim 5, Williams does not expressly teach an output scaling stage to compensate for scaling of stages due to bit growth at the corresponding stage as claimed in the application claim.

In column 4, lines 10-35, referring to figure 2, the third-adder (50) output potentially consists of nineteen bits, so it would seem logical for its output bits sent to the inter-pass memory 32 for use in the next pass of the FFT calculation to be only the most-significant eighteen bits. Hence, a selection circuit 52 allows the user to select the least-significant eighteen bits for storage in the inter-pass memory 32. In view of that, the selection circuit 52 performs equivalent bit growth compensation at output of the third adder to provide a desirable scaled output. Therefore, a person of ordinary skill in the art would have recognized the interchangeability of the selection circuit 52 as taught in Williams invention for the output scaling stage claimed in the application claim. The selection circuit 52 selects the least-significant eighteen bits for compensating potential bit growth at the output of third-adder 50.

Regarding claim 6, Williams does not expressly teach a signal analyzer as set forth in the application claim. However, as recited in claim 1, a bit-growth detector 39 (shown in both figures 2 and 4) monitors the inputs to the inter-pass memory 32 as to keep track of the largest value applied during any given pass. In column 3, lines 20-35, further teachings disclose the bit-growth detector 39 monitors the number of sign bits of all the values that enter the stage memory 32 in a given FFT pass and keeps track of

the lowest number of sign bits for any input. The bit-growth detector 39 then controls the shifter 38 to shift all multiplicands by one less than the lowest number of bits observed in any stage. In light of the aforementioned teachings, the bit-growth detector 39 effectively performs scaling at the processing stages experiencing bit growth. Therefore, a person of ordinary skill in the art would have recognized the interchangeability of the bit-growth detector 39 as taught in Williams invention for the signal analyzer claimed in the application claim.

Regarding claim 16, claim 16 is rejected on the same ground as for claim 1 because similar scope. Furthermore, referring to figure 1, the receiver includes a wide-band digital tuner 12, which corresponds to the claimed front-end portion for receiving data encoded in time domain, and a channelizer 16 which takes the form of fast Fourier transform butterfly circuit as disclosed in figure 4. Hence, channelizer 16 corresponds to the claimed digital signal processor. The butterfly circuit shown in figure 4 further includes a bit growth detector 39 for monitoring the inputs to the inter-pass memory 32 so as to keep track of the largest value applied during any given pass; see column 2 line 65 via column 5 line 15. In view of that, the step of monitoring the inputs to the inter-pass memory 32 corresponds to the claimed step of "analyzing the general consistent format of the time domain data signals".

Williams, however, does not teach a modem comprising elements as set forth in the application claim. Nevertheless, as well known in the art, modem is a

transceiver and a base station as discussed in figure 1 is also a transceiver. In view of that, it would have been obvious for one of ordinary skill in the art at the time of invention that the teachings of figure 1 can be modified to apply to a modem as claimed in the application claim.

Regarding claim 17, as discussed in column 4, lines 20-35, the design of prior art figure 2 is to maximize accuracy by using bit shifting to take advantage of as many of the circuit's bit position as possible. Because designing a circuit would involve in modeling and simulation, one of ordinary skill in the art will recognize that prior art teachings would model and simulate the format input before actually implement the butterfly circuit.

Regarding claim 18, as recited in claim 16, the butterfly circuit shown in figure 4 further includes a bit growth detector 39 for monitoring the inputs to the inter-pass memory 32 so as to keep track of the largest value applied during any given pass. In column 3, lines 20-35, the bit-growth detector 39 monitors the number of sign bits of all the values that enter the stage memory 32 in a given FFT pass and keeps track of the lowest number of sign bits for any input. It controls the shifter 38 to shift all multiplicands by one less than the lowest number of bits observed in any stage. In view of that, the bit-growth detector 39 performs equivalent function of the claimed signal analyzer.

Regarding claim 19, the base station in figure 1 is a wireless base station.

Regarding claim 21, claim 21 is rejected on the same ground as for claim 6 because of similar scope.

Regarding claim 22, as recited in claim 18, the butterfly circuit shown in figure 4 further includes a bit growth detector 39 for monitoring the inputs to the inter-pass memory 32 so as to keep track of the largest value applied during any given pass. Inputs of each pass are results of summation of input magnitudes for N points of the digitized signal through processing stages as shown in figure 4.

3. Claims 8-10, 14-15, 26-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vandenameele-Lepla US Patent Publication 2003/0058787 A1 in view of Williams U.S. Patent 5,717,620.

Regarding claims 8-9, in paragraph [0013], Vandenameele-Lepla teaches that in multi-carrier data communication systems such as OFDM, channel equalization is accomplished by first estimating and then compensating for the channel frequency response at the receiver end.

In paragraph [0006], Vandenameele-Lepla teaches that a subset of the plurality of time-domain signals includes training symbols that are embedded into the data for channel estimation purposes. In paragraph [0007], a correlator received the training sequence embedded in the multi-carrier time domain-signal by correlation process. In view of that, the correlator would perform an equivalent function of the claimed training tone extractor.

In paragraph [0013], an initial set of frequency-domain channel estimates are derived by dividing the received frequency-domain signals by their corresponding frequency domain training symbols. The initial frequency-domain channel estimates go through an IFFT and are transformed into time domain.

A weighting matrix that accounts for the finite time response of the channel and the position of the sub-carriers in the frequency domain is then processed in time domain to determine the maximum likelihood time domain estimates. This is then followed by an FFT to produce frequency domain channel estimates with reduced noise that are fed back to the equalizer.

Vandenameele-Lepla does not teach a channel estimator comprising the elements discussed above as claimed in the application claim. Since Vandenameele-Lepla teaches the method for channel equalization performing the aforementioned steps, one of ordinary skill in the art that at the time of the invention would have been motivated to implement a channel estimator including all components as discussed above.

Vandenameele-Lepla does not teach a Fast Fourier Transform component as set forth in the application claim. Nevertheless, the Fast Fourier Transform component is discussed in claim 1 rejection in view of Williams. As suggested in Vandenameele-Lepla invention, in paragraph [0022], the teachings result in significant reduction in complexity in channel equalization. Furthermore, Williams fast Fourier transform butterfly circuits apply to digital processing for channelizing a wide band radio signal. Therefore, it would have been obvious for one of

ordinary skill in the art that at the time of the invention that Vandenameele-Lepla FFT can be modified to implement Williams fast Fourier transform butterfly circuits. The modification is obvious because Williams FFT butterfly circuit performs a reduced Fast Fourier Transform with processing stages that compensates for bit growth and Vandenameele-Lepla teachings result in significant reduction in computational complexity.

Regarding claim 10, in column 2, lines 25-53, Williams discusses the butterfly circuit is radix 4 butterfly circuit. However, Williams further discloses that although there is a certain computational advantage to employing a radix-4 butterfly, those skilled in the art will recognize that the teachings are applicable to other radices, too. In light of the foregoing teachings, the plurality of processing stages as shown in figure 2 of Williams invention apply to $Log_2(N)$ number of radix-2 stages.

Regarding claim 14, Vandenameele-Lepla teachings apply to multi-carrier data communication systems such as OFDM.

Regarding claim 15, in column 1, lines 9-26, as discussed in Williams invention, it becomes practical to employ digital signal processing for channelizing a wide-band radio signal for de-multiplexing multiple frequency-division-multiplexed channels by fast-Fourier transformation. In light of that, one of ordinary skill in the art would have been

motivated to include the butterfly circuit as shown in figure 4 as part of a digital signal processing chip.

Regarding claim 26, claim 26 is rejected on the same ground as for claim 9 because of similar scope.

Regarding claim 27, claim 27 is rejected on the same ground as for claim 9 and further in view of claim 1 because of similar scope.

Regarding claim 28, Vandenameele-Lepla teachings apply to multi-carrier data communication systems such as OFDM and the channel impulse response has a finite duration impulse response as appreciated by one of ordinary skill in the art.

Regarding claim 29, claim 29 is rejected on the same ground as for claim 6 because of similar scope.

Allowable Subject Matter

4. Claims 7, 11-13, 25 and 30-31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nafie et al. U.S. Patent 6,320,902 B1 discloses "Time Domain Equalizer for ADSL".

Chun et al. U.S. Patent 6,101,230 discloses "Sampling Clock Signal Recovery Device And Method In Receiving Terminal OF DMT System".

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT

Khanh cong Tran 05/13/2005

Examiner KHANH TRAN